Please rewrite the Abstract as follows:

~~A high performance microprocessor system using instruction groups is disclosed herein.~~ The microprocessor system includes a central processing unit, memory, and a bus connecting the central processing unit and memory. An instruction fetching unit, connected to the bus, is provided for fetching instruction groups from the memory for use by the central processing unit and for storage within an instruction register. An instruction supplying unit operates to supply, in succession from the instruction register to the central processing unit, one or more instructions from each of the instruction groups. The system further includes an instruction decoder for configuring the instruction supplying unit to select, from the instruction register, operands associated with instructions from particular instruction groups--.

IN THE CLAIMS

Please amend claims 71-75 and 77-85 as follows:

71(Amended). A microprocessor system comprising:

a central processing unit;

memory;

a bus connecting said central processing unit to said memory;

instruction fetching means that are connected to said bus to fetch [instructions] instruction groups [for said central processing unit on] via said bus from said memory, each of said instruction groups including at least one instruction;

an instruction register for receiving a first of said [fixed-length] instruction groups from said instruction fetching means, said first of said [that] instruction groups including [consist of multiple] one or more sequential instructions [from said bus from said instruction fetching means];

instruction supplying means [that are connected to said instruction register] for supplying, in succession from said instruction register, said [multiple] one or more sequential instructions of said first of said instruction groups [in succession from said instruction register] to said central processing unit;